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13. ABSTRACT *(Maximum 200 words)*

This report contains research results in the areas of in-situ rapid isothermal processing, in-situ cleaning of semiconductor surfaces, solid phase epitaxial growth of II-A fluorides, in-situ metallization, the role of thermal stress, use of II-A fluorides as buffer layers for the decompostion of high temperature superconducting thin films and the set up of RIP assisted MOCVD.

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1. R. Singh, R.P.S. Thakur, A. Katz, A.J. Nelson, S.C. Gebhard, and A.B. Swartzlander, "Relationship Between Thermal Stress and Structural Properties of SrF_2 Films of (100) InP," Appl. Phys. Lett (In Press).

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8. SCIENTIFIC PERSONNEL SUPPORTED BY THIS PROJECT AND DEGREES AWARDED DURING THIS REPORTING PERIOD:

1. R. Singh, University of Oklahoma.
2. F. Radpour, University of Oklahoma.
3. R.P.S. Thakur, University of Oklahoma.
4. J. Narayan, North Carolina State University.
5. A.R. Srivasta, North Carolina State University, PhD, 1989.

6. William Krisa, University of Oklahoma, M.S., 1988.

I. INTRODUCTION

The original purpose of this three year project was to develop a low temperature processing technique for the deposition of Si/CaF_2 structure on Si substrate that can be used to realize advanced Si CMOS and bipolar circuits. However, after the first year at the direction of ARO the emphasis was changed from Si to InP substrates. Also at the end of the second year, this project was reduced from three years to only two years (reduced budget in second year). Thus, the project was not funded for the proposed three years. However, the project has been extremely successful, as is evident from the research result described here.

II. SUMMARY

A. IN-SITU RAPID ISOTHERMAL PROCESSING

For the first time, we have assembled an ultra high vacuum in-situ rapid isothermal processor. The in-situ rapid isothermal processor consists of an ultra high vacuum system coupled to a rapid isothermal processor. The in-situ rapid isothermal processor has the capability of in-situ cleaning of semiconductor surface, thermal or electron beam deposition and in-situ annealing of materials. The concept and the system developed in our laboratory can be used in the single wafer reduced thermal budget integrated manufacturing of micro, opto and cryo electronic devices and circuits. The system cost is much lower compared to individual deposition and annealing systems. Details of the system are described in reference 1. B. IN-SITU CLEANING OF SEMICONDUCTOR SURFACE

Based on rapid isothermal processing, we have developed a new reduced thermal budget (product of processing time and temperature) processing technique for the cleaning

of semiconductor surface. The technique involves heating the substrate for short periods in the presence of 5% H_2 and 95% Ar mixture. Excellent quality of interface was obtained, as was observed by TEM and auger depth profile. Details of silicon and InP surface cleaning are described in reference 1 and 2 respectively.

C. SOLID PHASE EPITAXIAL GROWTH OF II-A FLUORIDES

For the first time, we have grown II-A fluorides (CaF_2, BaF_2, SrF_2 and their mixture) by solid phase epitaxial growth. The process involves in-situ cleaning, room temperature deposition of II-A fluoride followed by in-situ annealing. The II-A fluoride films obtained by solid phase epitaxial approach are of excellent quality. Details of the preparation and characterization of the films are described in reference 1 to 5.

D. IN-SITU METALLIZATION

Generally, metallization and annealing are done in separate systems. For the first time, we have shown that in-situ annealing after metallization can provide improved quality of ohmic contacts compared to their ex-situ annealed counter partners. These results are described in reference 6.

E. ROLE OF THERMAL STRESS

The thermal stress plays a critical role in determining the structural and electrical properties of the thin films. We have studied the correlation between thermal stress and the structural properties. II–A fluoride films deposited at room temperature followed by in–situ annealing provide less thermal stress compared to the ex–situ annealed films and also show lower thermal hystersis for the same thermal budget. The ex–situ annealed films are full of defects and are polycrystalline in nature. Thus we have found a direct

correlation between the structural properties and the thermal stress [4, 7].

F. USE OF II–A FLUORIDES AS BUFFER LAYER FOR THE DEPOSITION OF HIGH TEMPERATURE SUPERCONDUCTING THIN FILMS

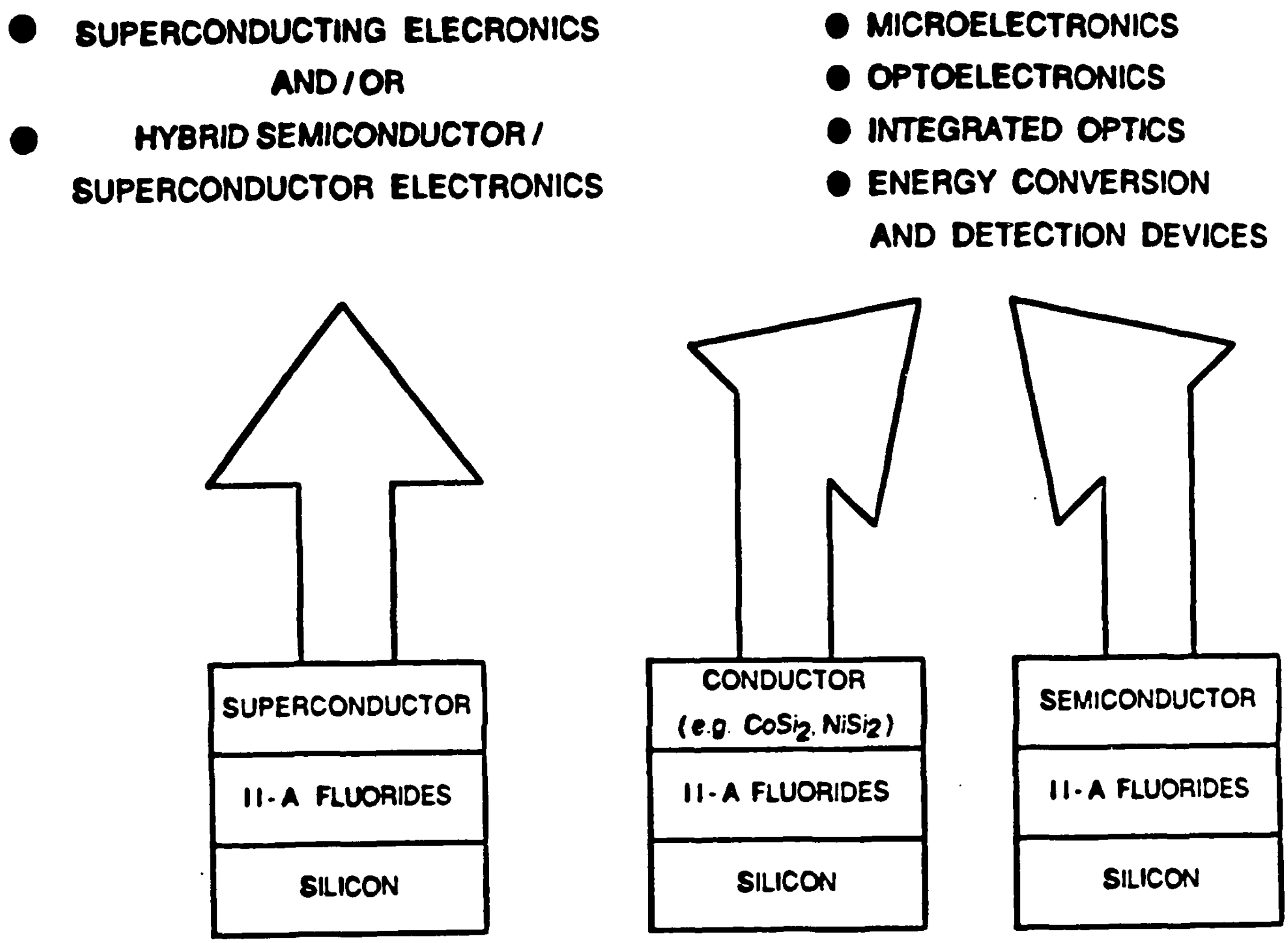
We have used buffer layer BaF_2 to deposit thin films of Y–Ba–Cu–0 on Si and other substrates [8–10]. The capability of depositing high temperature superconducting thin films on Si substrates [8, 10], coupled with already demonstrated capability of semiconductor–II–A–fluoride–silicon hetrostructure suggest the possibility of integration of diverse technology on the silicon or some other common substrate (Fig. 1 and 2).

G. SET UP OF RIP ASSISTED MOCVD

We have setup an RIP assisted MOCVD system for the deposition of InP on silicon substrate. The system has the capability of in–situ rapid isothermal cleaning of silicon, InP and other semiconductor surfaces. A buffer layer of II–A fluorides can be deposited by RIP MOCVD system [11]. For the deposition of InP, we plan to use tertiary butyl phosphine and tri methyl indium as the precursors. In–situ surface study can be carried out by RHEED. The system will be operational by the end of next month.

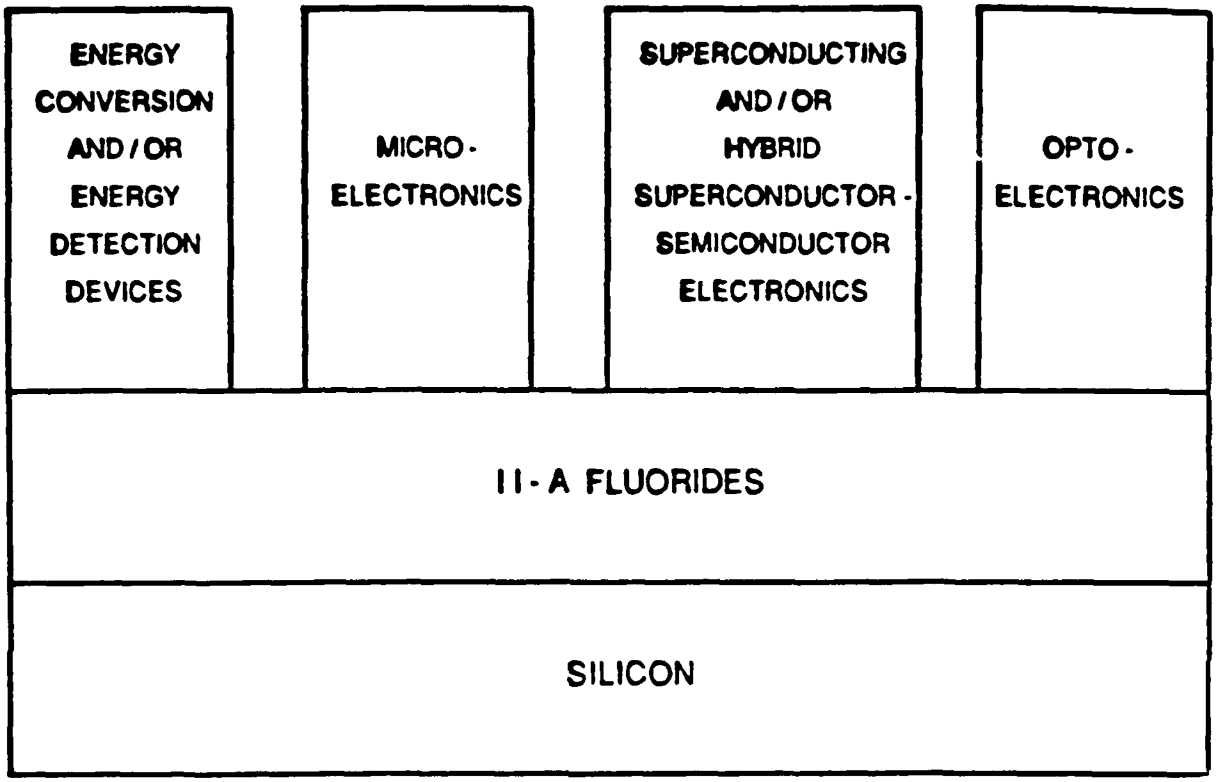
It is worth mentioning here that for the similar or lower substrate temperature and smaller thermal budget, than furnace processing, the use of ultraviolet and visible photons in the rapid isothermal processing provide improved quality of materials [12]. Thus, even at lower substrate temperatures and long–time heating, RIP has advantages over furnace processing.

Fig. 1



ROLE OF EPITAXIAL FLUORIDES IN THE DEVELOPMENT OF VARIOUS ELECTRONIC AND OPTICAL DEVICES AND CIRCUITS.

Fig. 2



EPITAXIAL MATERIALS BASED SUPERCHIP INTEGRATING DIVERSIFIED TECHNOLOGIES

III. FUTURE PLANS

We propose to deposit InP on II–A fluoride/Si structure by RIP assisted MOCVD. The InP on silicon technology is of great importance, both for micro and opto electronics. As a test structure, we plan to demonstrate the feasibility of ultra high performance three terminal devices by using reduced thermal budget InP on Si technology.

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APPENDIX - SELECTED PUBLICATIONS